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Design of Leakage Power Reduced Static RAM using LECTOR

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***Abstract*— The scaling down of technology in CMOS circuits, results in the down scaling of threshold voltage thereby increasing the sub-threshold leakage current. LECTOR is a technique for designing CMOS circuits in order to reduce the leakage current without affecting the dynamic power dissipation, which made LECTOR a better technique in leakage power reduction when compared to all other existing leakage reduction techniques. This paper presents the analysis for leakage current in Static RAM implementing LECTOR technique using 45nm technology.**

***Keywords*— Low Power, Sub-threshold leakage current, Self-controlled LCTs, Transistor stacking, Deep-submicron**

I. INTRODUCTION

To achieve high density and high performance, CMOS technology feature size and threshold voltage have been scaling down for decades. Because of this trend, transistor leakage power has increased exponentially. High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The main factor in the leakage power is the sub-threshold leakage current which increases as the channel length of the MOSFET decreases. Thus to achieve low power performance, lowering the supply voltage is the most effective way as the dynamic power varies as the square of supply voltage and the leakage power varies linearly with supply voltage. But it results in drastic degradation of performance by reducing the supply voltage and keeping the threshold voltage at its original value, because as the supply voltage is reduced the gate drive voltage (V_{DD}-V_T) reduces and thus the delay increases, since propagation delay in a CMOS gate is approximated as

$$T_d = \frac{C_L V_{DD}}{(V_{DD} - V_T)^{\alpha}}$$

α is small positive constant used to that models the short channel effects.

To overcome the performance degradation, threshold voltage (V_T) is to be reduced. Reduction in threshold voltage causes an exponential increase in sub-threshold leakage current, thereby static power. As one continues to scale down supply voltage and threshold voltage, the increased leakage power can dominate the dynamic switching power. In 22nm technology, the static power dissipated is 70-72% of the total power dissipated, where the supply voltage is 0.8V.

In this paper LECTOR technique is implemented on memory circuit i.e., Static RAM for 1-bit and 512-bit.

II. RELATED WORK

There are numerous methods proposed to control leakage power dissipation. Power gating is one of the techniques proposed for leakage reduction, which turns off the device by cutting OFF the supply voltage. In this technique bulky NMOS and/or PMOS device called sleep transistor is used in a path between supply voltage and ground. This is done to create virtual power and ground rails in the circuit. This technique creates a negative effect on the circuit switching speed when the circuit is operating in active mode. The identification of the idle regions of the circuit and the generation of the sleep signal need additional hardware capable of predicting the circuit states accurately. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors.

A technique makes use of the dependence of the leakage current on the input vector to the gate. With additional control logic, the circuit is put into a low-leakage standby state when it is idle and restored to the original state when reactivated. Reactivation state forces the need to remember the original state information before going to low-leakage standby state. This requires special latches, thereby increasing the area of the circuit by about five times in the worst case. Also, the amount of time for which the unit remains in idle state should be long enough so that the dynamic power consumed in forcing the circuit to low-leakage state and the leakage power dissipated in the standby state together is less than the leakage power without the technique.

The use of multiple threshold voltage CMOS (MTCMOS) technology for leakage control is another technique. The transistors of the gates are at low threshold voltage and the ground is connected to the gate through a high-threshold voltage NMOS gating transistor. The logical function of a gating transistor is similar to that of a sleep transistor. The existence of reverse conduction paths tend to reduce the noise margin or in the worst case may result in complete failure of the gate. Moreover, there is a performance penalty since high-threshold transistors appear in series with all the switching current paths. A variation of MTCMOS technique is the Dual V_T technique, which uses transistors with two different threshold voltages. Low-threshold transistors are used for the gates on the critical path and high-threshold transistors are used for those not in the critical path. In both MTCMOS and Dual V_T methods, additional mask layers for each value of threshold voltage

are required for fabricating the transistors selectively according to their assigned threshold voltage values. This makes the fabrication process complex.

The techniques discussed above suffer from turning-on latency, that is, when the idle subsections of the circuit are reactivated, they cannot be used immediately because some time is needed before the sub-circuit returns to its normal operating condition. The latency for power gating is typically a few cycles, and for Dual V_T technology, is much higher. Also, these techniques are not effective in controlling the leakage power when the circuit is in active state.

Forced stacking introduces an additional transistor for every input of the gate in both N- and P-networks. This ensures that two transistors are OFF instead of one for every OFF-input of the gate and hence makes a significant savings on the leakage current. However, the loading requirement for each input introduced by the forced stacking reduces the drive current of the gate significantly. This results in a detrimental impact on the speed of the circuit.

The sleepy stack technique has a structure merging the forced stack technique and the sleep transistor technique. When applying the sleepy stack technique, each existing transistor is replaced with two half sized transistors and add one extra sleep transistor. The leakage reduction of the sleepy stack structure occurs in two ways. First, leakage power is suppressed by high-Vth transistors, which are applied to the sleep transistors and the transistors parallel to the sleep transistors. Second, two stacked and turned off transistors induce the stack effect, which also suppresses leakage power consumption. By combining these two effects, the sleepy stack structure achieves ultra-low leakage power consumption during sleep mode while retaining exact logic state. The price for this, however, is drastically increased area. And the major disadvantage of having controlling circuitry for sleep transistors is also carried here. As the sleep transistors are bulky, hence increases the dynamic power.

Sleepy Keeper is a better leakage reduction technique compared to sleepy stack. It gives an excellent alternate for sleepy stack in terms of reducing the area overhead since it doesn't need three transistors to be replaced to one transistor. Sleep transistors are connected to the circuit along with NMOS connected to Vdd and PMOS connected to Gnd. The sleep transistor is turned on when the circuit is active and turned off when the circuit is in idle state with the help of sleep signal. This creates virtual power and ground rails in the circuit. Hence, there is a significant detrimental effect on the switching speed when the circuit is active. The identification of the idle regions of the circuit and the generation of the sleep signal needs an additional hardware capable of predicting the circuit states accurately, thereby increasing the area requirement of the circuit. This technique creates a negative effect when the circuit is operating in active mode in terms of the circuit performance. This additional hardware consumes power throughout the circuit operation even when the circuit is in an idle state to continuously monitor the circuit state and control the sleep transistors.

In this work, a new technique for leakage control in CMOS circuits is developed. The proposed technique avoids the problems associated with all the above discussed techniques.

III. LECTOR TECHNIQUE

LECTOR approach for reduction of leakage power is based on the effective stacking of transistors in the path from supply voltage to ground. The basic idea behind LECTOR is based on the concept that "a state with more than one transistor OFF in a path from supply voltage to ground is far less leaky than a state with only one transistor OFF in any supply to ground path." In this method, two leakage control transistors (LCTs) were introduced in each CMOS gate, a PMOS (LCT1) added to the pull-up network and a NMOS (LCT2) added to the pull-down network and the gate terminal of one LCT is controlled by the source terminal of the other, such that one of the LCTs is always *near its cutoff* region of operation for any input(s) given to the CMOS gate, thus providing additional resistance in the path from supply to ground, decreasing the sub-threshold leakage current, thereby the static power. This section illustrates Leakage Control TransistOR (LECTOR) technique with the case of memory circuits and other CMOS logic circuits.

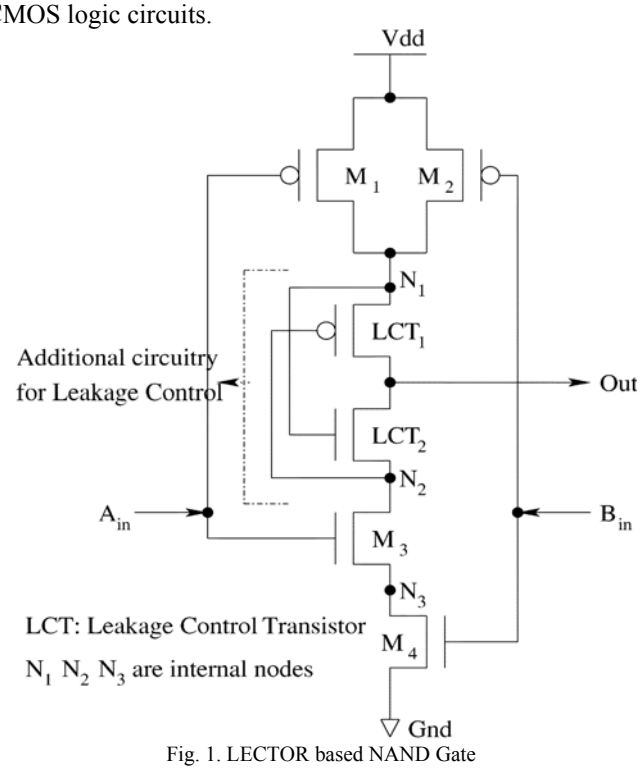

Fig. 1. LECTOR based NAND Gate

A CMOS NAND gate with the addition of two leakage control transistors which is known as LECTOR NAND is shown in Fig. 1. Two leakage control transistors LCT1 (PMOS) and LCT2 (NMOS) are introduced between the nodes N1and N2 of the pull-up and pull-down logic of the NAND gate. The drain nodes of the transistors LCT1 and LCT2 are connected together to form the output node of the NAND gate. The source nodes of the transistors are connected to nodes N1 and N2 of pull-up and pull-down logic, respectively. The switching of transistors LCT1 and LCT2 are controlled by the voltage potentials at nodes N2

and N1 respectively. This wiring configuration ensures that one of the LCTs is always *near its cutoff region*, irrespective of the input vector applied to the NAND gate. This can be seen from the dc characteristics shown in Fig. 2 (a) and 2 (b).

TABLE I
LCT NAND STATE MATRIX

Transistor Reference	Input Vector – (A_{in}, B_{in})			
	(0,0)	(0,1)	(1,0)	(1,1)
M1	On state	On state	Off state	Off state
M2	On state	Off state	On state	Off state
LCT1	Near Cut-Off state	Near Cut-Off state	Near Cut-Off state	On state
LCT2	On state	On state	On state	Near Cut-Off state
M3	Off state	Off state	On state	On state
M4	Off state	On state	Off state	On state

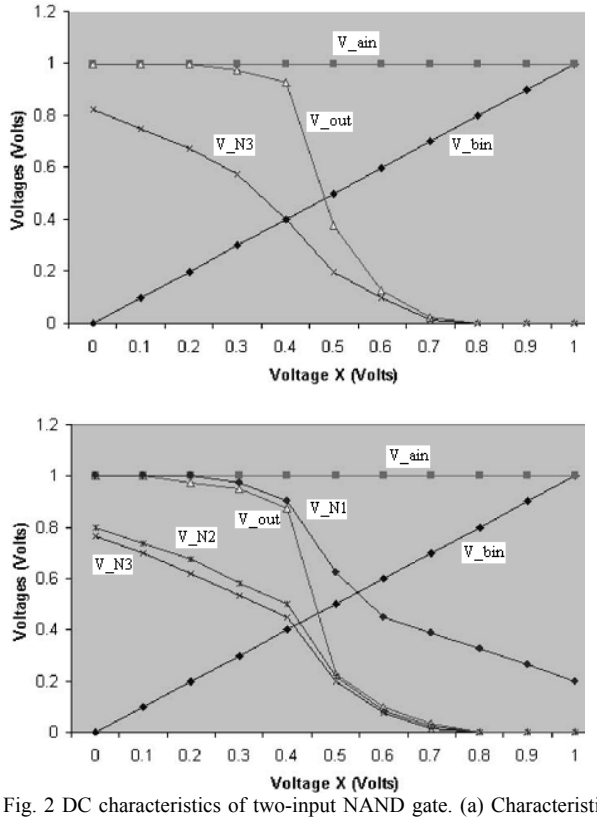

Fig. 2 DC characteristics of two-input NAND gate. (a) Characteristics of basic NAND gate (b) Characteristics of LCT NAND gate.

It can be observed that the output voltage variation is similar in both the cases.

Consider the dc characteristics of the LCT NAND gate. When A_{in} = 1V and B_{in} = 0V, the voltage at the node N2 is 800 mV. This voltage is not sufficient to turn LCT1 completely to OFF state. Hence, the resistance of LCT1 will be lesser than its OFF resistance, allowing conduction. Even though the resistance of LCT1 is not as high as its OFF state resistance, it increases the resistance of Vdd to ground path, controlling the flow of leakage currents, resulting in leakage power reduction. Similarly, when A_{in} = 1V and B_{in} = 1V, the voltage of node N1 is 200 mV, operating the transistor LCT2 near its *cutoff* region. The states of the transistors for all possible combinations of input vectors for the LCT NAND gate are tabulated in Table I.

Thus, the introduction of LCTs increases the resistance of the path from Vdd to ground. This also increases the propagation delay of the gate. To reduce this hostile effect, the transistors of LCT gate are sized such that the propagation delay is equal to its conventional counterpart.

IV. STATIC RANDOM ACCESS MEMORY

The 1-bit Static RAM design using 6 transistors is shown in the Fig. 3. Static RAM is a power-hungry circuit, since it should be in active mode continuously.

Hence in nanoscale technology, the leakage power in Static RAM will be comparatively very high than other CMOS circuits. Using other peripheral circuitry like sense amplifiers, precharge circuit and row decoders, the LECTOR technique is applied to higher capacity SRAM.

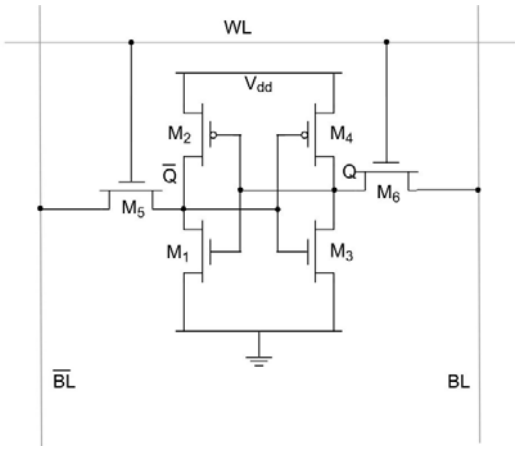

Fig. 3 One-bit SRAM Cell

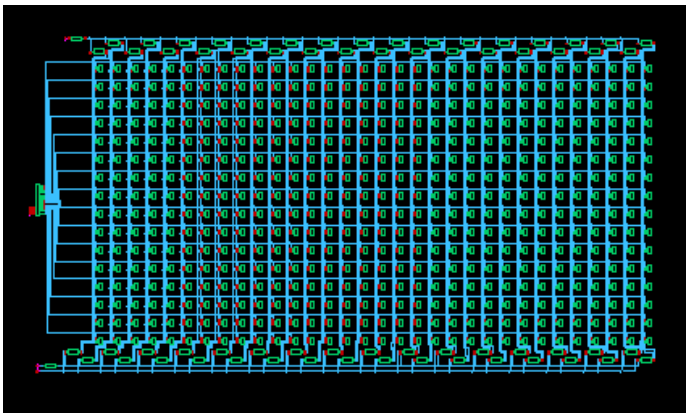

Fig. 4 512-bit SRAM cell

TABLE III
RESULTS FOR STATIC RAM USING 90 AND 45 NM TECHNOLOGY

SRAM	Technology	Leakage power (W)		%age decrease in power dissipation
		Conventional	LECTOR	
1-bit	90nm	8.99E-09	6.21E-09	30.928
	45nm	5.15E-06	3.28E-06	36.304
512-bit	90nm	46.82E-03	6.90E-03	85.269
	45nm	99.36E-03	51.36E-03	48.312

The one bit Static RAM cell along with a 4 to 16 decoder, precharge circuit and write driver is used to obtain the 512 bit Static Random Access Memory. 16X32 array arrangement is used to obtain the half-Kb SRAM as shown in Fig. 4. As there are 32 columns, for each column, there will be a precharge circuit and a write driver. The precharge circuit is used to pull the bit line and bit line bar during the read operation. The LECTOR implementation is done to obtain the leakage reduction in the deep submicron technologies.

V. EXPERIMENTAL RESULTS

The HSPICE simulator is used to measure the leakage power. Table II shows the results obtained through the technique for the Static RAM for 1-bit and 512-bit. Also these results are compared with that of the respective conventional case.

VI. CONCLUSIONS

The scaling down of device dimensions, supply voltage, and threshold voltage for achieving high performance and low dynamic power dissipation has largely contributed to the increase in leakage power dissipation. With deep-submicron and nanometer technologies, the leakage current becomes more critical in portable systems where battery life is of primary concern.

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. This paper presents "LECTOR" to tackle the leakage problem. LECTOR uses two additional self-controlled transistors. Like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, LECTOR also achieves leakage power reduction but with the advantage of not affecting the dynamic power as this technique does not require any additional control and monitoring circuitry like in and also maintains exact logic state.

LECTOR technique can retain logic state, so it can be used for both generic logic circuits as well as memories, i.e., SRAM. When applied to Static RAM, the LECTOR technique achieves up to 35-50% leakage reduction over the conventional circuit without affecting the dynamic power.

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